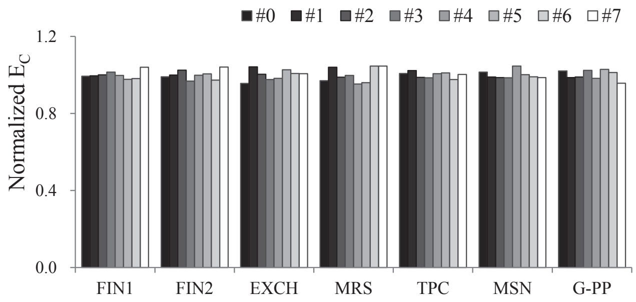

Fig. 3. Normalized erase count (E_C)

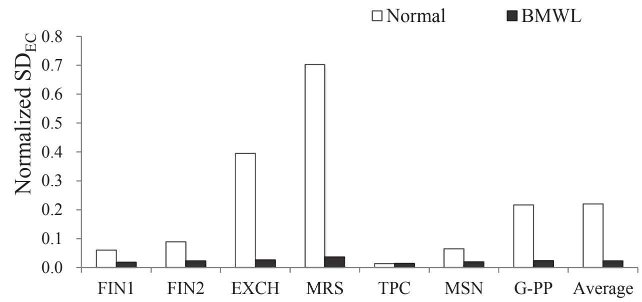

Fig. 4. Standard deviation of normalized erase count (SD_{EC})

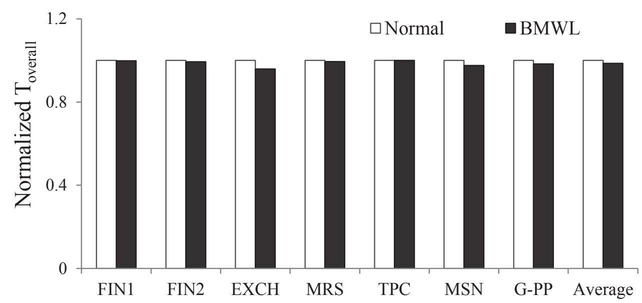

Fig. 5. Normalized overall throughput ($T_{overall}$)

In Fig. 2, we assume that NFM_6 and NFM_7 have maxE_c and minE_c respectively. In this situation, the proposed method redirects the write request, which is originally directed to NFM_6, to NFM_7. If data with same logical page address in NFM_6 exist, the data should be moved to NFM_7 after being temporarily stored in NFM controller, which requires additional time for data transfer. Nevertheless, as shown in the following experiment result, the overhead is negligible thanks to faster data transfer speed and a partial data update of modern NFMs.

III. Evaluation

To evaluate the effectiveness of the proposed method, we implemented a trace-driven simulator that consists of a page-level FTL [3], the specification of NFM [4] and the configurations of storage system. Various workloads are collected from [5] (FIN1, FIN2), [6] (EXCH, MRS, TPC, MSN) and by DiskMon [7] (G-PP) during daily PC use.

Fig. 3, 4 and 5 shows performance of the proposed method, which is compared to the baseline which does not consider multi-chip wear-leveling ($Normal$). As shown in Fig. 3, the proposed $BMWL$ maintains balanced E_c regardless of workloads in contrast Fig. 1. Quantitatively, in Fig. 4, standard deviation of normalized erase count (SD_{EC}) of $BMWL$ is 20 times smaller than $Normal$ in EXCH and MRS. On average, $BMWL$ reduces SD_{EC} and maxE_c by 90% and 20% respectively, which means that the proposed method not only improves the life-time balance of individual NFMs but also improves overall life-time of NFSD.

Fig. 5 shows overall throughput ($T_{overall}$) of $BMWL$ and $Normal$. Although $BMWL$ requires additional data transfer when redirecting write requests, the overhead of $BMWL$ is only 1% for the compensation of significant improvement of life-time. The small overhead comes from faster data transfer speed up to 200MB/s.

IV. Conclusion

This paper proposes a wear-leveling method that improves overall life-time of a NFSD consisting of multiple NFMs. For balanced E_c of all NFMs, the proposed method monitors E_c of multi-chip and redirects write from an imbalanced NFM to another. In experiment, the proposed method greatly improves overall life-time of NFSD through balanced E_c of multi-chip. Additionally, the proposed method can be modified to compensate a deviation of life-time deviation occurred by the processing variation of NFMs.

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References

[1] J.-U. Kang, J.-S. Kim, C. Park, H. Park, and J. Lee, "A multi-channel architecture for high-performance nand flash-based storage system," *Journal of Systems Architecture*, vol. 53, no. 9, pp. 644–658, 2007.

[2] S.-H. Park, S.-H. Ha, K. Bang, and E.-Y. Chung, "Design and analysis of flash translation layers for multi-channel nand flash-based storage devices," *Consumer Electronics, IEEE Transactions on*, vol. 55, no. 3, pp. 1392–1400, 2009.

[3] H.-j. Kim and S.-g. Lee, "A new flash memory management for flash storage system," in *Computer Software and Applications Conference, 1999. COMPSAC'99. Proceedings. The Twenty-Third Annual International*. IEEE, 1999, pp. 284–289.

[4] *Micron Technology, NAND Flash Memory Datasheet, MT29FXXG08AXXXX.*

[5] *UMass Trace Repository, http://traces.cs.umass.edu/.*

[6] *Storage Networking Industry Association, http://iotta.snia.org/.*

[7] *DiskMon for Windows v2.01, http://technet.microsoft.com/en-us/sysinternals/bb896646.aspx, 2010.*